REMARKS

The above-referenced patent application has been reviewed in light of the Office Action of June 10, 2004. Reconsideration of the above-referenced patent application in view of the amendments and remarks is respectfully requested. No claims have been amended, added or canceled.

RESPONSE TO 35 U.S.C. §103 REJECTION

The Examiner rejected claims 1, 3-7, 11-14, 16-21, 25-26, 28, 29, 32, 34 and 35 under 35 U.S.C. §103(a) as being unpatentable over Ibaraki (U.S. Patent No. 5,546,461) in view of Chapman (U.S. Patent No. 6,173,402), Faria (UK Patent Application GB 2316278A), Schneier (Applied Cryptography) and Dent.

Rejection of the claims is traversed. None of the references alone or in combination provides "scrambling the blocks of the digital video signal responsive to a key of which a remote computer number and a video position number are components, the video position number representing positional information including the block to be scrambled, the scrambling includes XOR operations between the blocks of the digital video signal to be scrambled and other operands, with each XOR operation being between one of the blocks to be scrambled and one of the other operands," as claimed in the claims.

Neither Ibaraki nor any of the other references teach or disclose the digital video to be scrambled taken a "block" at a time and then bit-XOR'ed with the "combined key." In particular, the present invention generates a "combined key" from an initial key and processor number. Each of the initial key and processor number first undergoes a hash (hash 1 and hash 2 respectively). The hashed values are then combined to form an N bit "combined key." The digital video to be scrambled is then taken a "block" at a time and then bit-XOR'ed with the "combined key." The result then undergoes another round of XOR'ing. This time, the bits are organized into byes and each byte is then XOR'ed with the least significant byte of the relative position of that byte in the video. The result then forms the scrambled video. This additional XOR'ing serves to further scramble the data bit further. In compression techniques such as MPEG in which there can be a sequence of 0's, without this additional scrambling stage, the combined key can be exposed. Furthermore, instead of using the least significant byte of the file

position, a hashed version of the byte can be used. Hashing here will then be dependent on the processor number.

Chapman also fails to teach or suggest scrambling the data a "block" at a time and then bit-XOR'ed with the "combined key." In particular, the present invention generates a "combined key" from an initial key and processor number. Chapman in fact teaches away from a combined key and scrambling a block at a time. An immutable value specific to the computer system is not a combined key. Chapman is also silent with respect to scrambling a block at a time.

Moreover, Faria, Schneier and Dent fail to correct the deficiencies of Ibaraki and Chapman. In the present invention, the digital video to be scrambled is taken a "block" at a time and then bit-XOR'ed with the "combined key." The result then undergoes another round of XOR'ing. This time, the bits are organized into byes and each byte is then XOR'ed with the least significant byte of the relative position of that byte in the video. The result then forms the scrambled video. This additional XOR'ing serves to further scramble the data bit further. None of the cited references disclose or suggest the above. All that is shown or indicated is the presence of an XOR circuit.

Even assuming, for the sake of argument, that the references teach the claimed language, which Applicants maintain the references do not, the references still fail to correct the deficiencies of Ibaraki. Applicants respectfully remind the Examiner that in determining the differences between the alleged prior art and the claimed invention the question for the Examiner is not whether "the differences themselves would have been obvious, but whether the invention as a whole would have been obvious." (emphasis in original). MPEP 2141.02 (citing Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530 (Fed. Cir. 1983). In making his rejection, the Examiner has relied upon references teaching of logical XORs to supplement the inadequate teachings of Ibaraki. However, as discussed above, Applicants assert that the Examiner has failed to properly read the limitations of claim 1 as reflects the claimed invention as a whole. Claim 1 clearly recites "scrambling the blocks of the digital video signal responsive to a key of which a remote computer number and a video position number are components, the video position number representing positional information including the block to be scrambled, the scrambling includes XOR operations between the blocks of the digital video signal to be scrambled and other operands, with each XOR operation being between one of the blocks to be scrambled and one of

the other operands." Thus, by considering Ibaraki's and Chapman's disclosure to be deficient for only failing to disclose "the use of logical OR'g (XOR) to create scrambling/de-scrambling data" the Examiner has failed to consider obviousness in the context of the claimed invention as a whole.

Applicants respectfully assert that the combination of Ibaraki with the other references fails to establish a *prima facie* case of obviousness. Applicants respectfully direct the Examiner's attention to MPEP 2143.01 wherein states that a *prima facie* case of obviousness can

> only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art (emphasis added)
>
> (citing In re Kotzab, 217 F.3d 1365 (Fed. Cir. 2000)).

Thus, Applicants respectfully assert that the Examiner has failed to adhere to the admonition that a *prima facie* case of obviousness can only be established by providing "some objective reason to combine the teachings of the references." MPEP 2143.01 (citing Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

In conclusion, Applicants maintain that the Examiner has failed to make a *prima facie* case of obviousness under 35 U.S.C. § 103, and it is therefore respectfully requested that the Examiner withdraw his rejection of the claims.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

No additional fees are required for claims.

The required fee for a three month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to Deposit Account No. 02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 12/10/04
Nedy Calderon Date